Reference Hardware Design Guideline

Ethernet Board

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1.0	May 25, 2020

Panasonic Corporation
Automotive Company R&D Division

Revision History

Date	Version	Comments
May 25, 2020	1.0	Initial Release

References

No.	Document Name	Version	Release Date
1	RH_Design_Control_ver.1.0.pdf	1.0	May 25, 2020
2	RH_Design_Vehicle_Audio_ver.1.0.pdf	1.0	May 25, 2020

Contents

Figures and Tables

1. Ethernet Board

Ethernet Board is connected to Control Board and performs interface conversions to enable high-speed communications between external devices. The SoC connection in this design uses one PCI-Express x2 channel and one USB3.0 SuperSpeed channel. However, the connection may vary depending on how the SoC is designed. Using the same wiring, another type of buses such as MII, can be connected in place of PCI-Express.

The design of Reference Hardware makes it possible to support a variety of SoCs. Reference Hardware in this document, in fact, is designed to meet the requirements of Renesas R-Car H3. (Hereinafter, it is referred to as “R-Car H3 Reference Hardware” and Reference Hardware using any other SoC is referred to as “Standard Reference Hardware”.)

1.1. Board Outline

The following figure shows Ethernet Board dimension. 1.2[mm] is the assumed board thickness. If the change is required, interference with other boards should be considered.

The interface to Control Board is a 60-pin board-to-board connector mounted on the solder side of Ethernet Board. The external interface connectors are also mounted on the solder side to avoid interference issues that may occur when assembled.

The spacing between the board and chassis is shown as below. External interface connectors are to be placed in the position relative to the chassis.

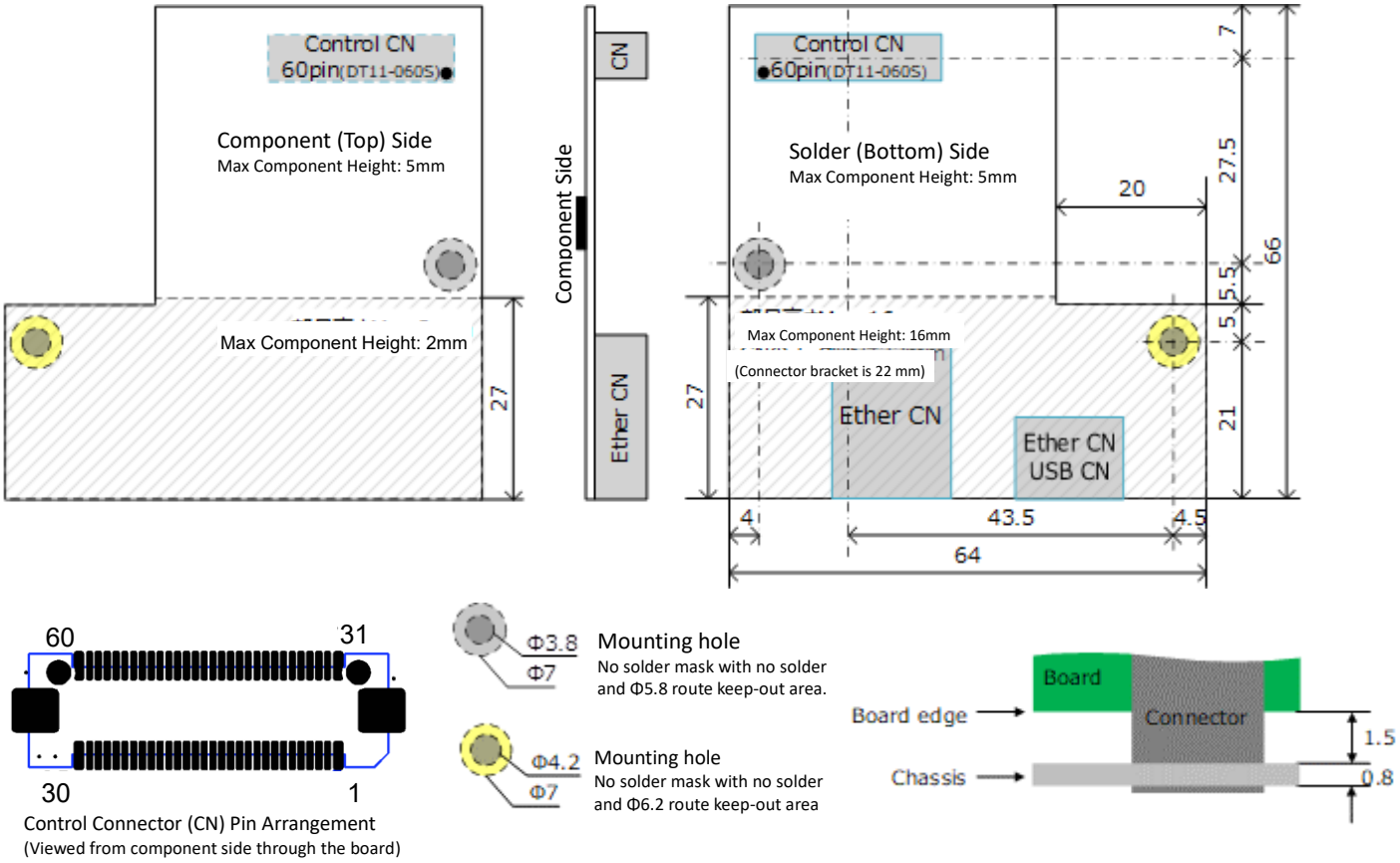


Figure 1 Board Dimension

When there is not enough space in Ethernet Board, the space of VideoIn0 Board can be added to expand Ethernet Board. The space of VideoIn0 Board used for the board expansion will no longer function as VideoIn0 Board but serve as a primary channel instead. Therefore, it is recommended to design the board in the size shown in Figure 1 as far as possible.

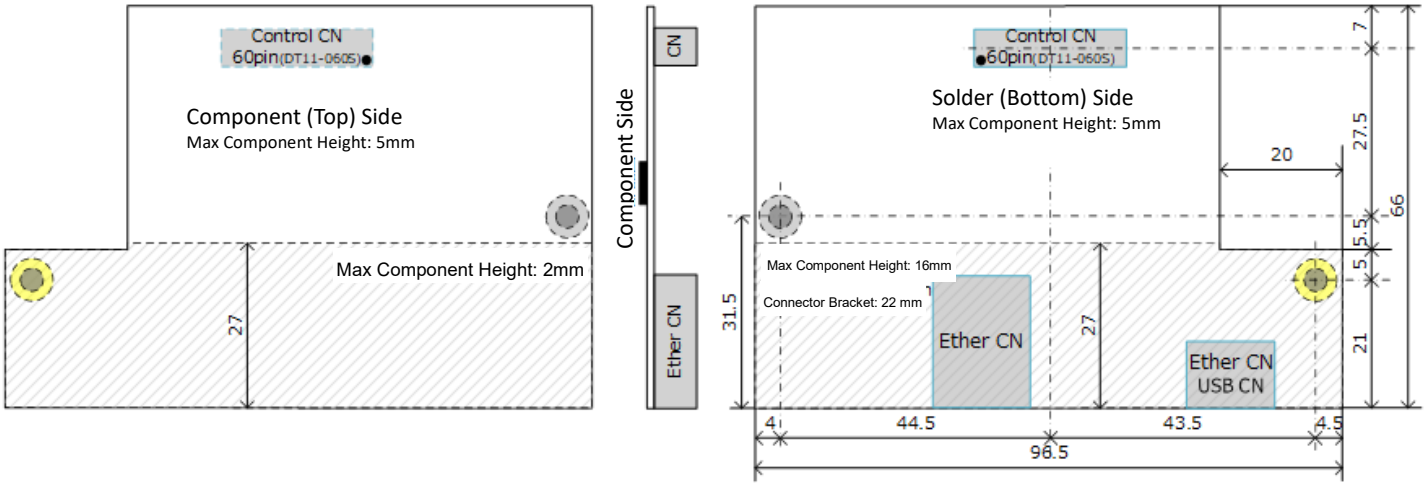


Figure 2 Expanded Board Dimension

1.2. Power Supply

There are five power supply rails that power Ethernet Board. The specification of each power supply is shown in Table 1.

Table 1 Ethernet Board Power Supply

Signal Name	Voltage Spec [V]			Current Limit per line [mA]	Description
	Min	Typ	Max		
VDD_5P8V		5.87		200	Pin 1, Pin 2 (2 pins)
VDD_3P3V		3.3		200	Pin 31, Pin 32 (2 pins)
VDD_1P8V		1.8		200	Pin 3, Pin 4 (2 pins)
IO_IF (VDD_USB_IOBANK)		3.3/1.8		50	Pin 52 (1 pin) Voltage depends on the power supply switch setting on Control Board (FPGA USB IO voltage) 3.3V is the default for R-Car H3 Reference Hardware.
VDD_ETH_CORE		1.2/1.5		200	Pin 33, Pin 34 (2 pins) Voltage depends on the power supply switch setting on Control Board (VIN Core voltage) 1.2V is the default for R-Car H3 Reference Hardware.

A power circuit can be built on Ethernet Board if no power source is available for an intended purpose.
Fire and smoke must be prevented integrating the protection into the power IC in the event of short circuit at the output side. The use of IC with OCP (overcurrent protection) is essentially required.

If necessary current is more than the specified limit, one of the possible solutions is to use another portion of the same power supply that is allocated to a different board with no power consumption (due to constraints towards other boards). Information about apportioned current for each power consumption can be found in the chapter of power supply configuration in *Design Guideline for Control Board*. Given that 400[mA] is the maximum of current rated for each pin of a connector, the overall current rating needs to be maintained based on the number of pins.

The details on power supply control are indicated in the schematics in this document and *Reference Hardware Design Guideline for Control Board and Vehicle/Audio Board*.

1.3. Board-to-Board Interface

60-pin board-to-board connector is used to connect Control Board to Ethernet Board. A receptacle connector (KEL DT01-060S) is assumed to be used on the side of Control Board, and a plug connector (KEL DT11-060S-10) is assumed to be used on the side of Ethernet Board.
These connectors are compliant with SATA Rev3.0 allowing 6[Gbps] physical transfer rate. The floating structure can accept misalignment of ±0.5 [mm] maximum in the directions of X and Y axis. Current rating per pin is 400[mA].

The voltage for signals interfacing with Control Board should be able to adjust to both 1.8[V] and 3.3[V] as Ethernet Board and USB Board uses signals of the same terminal voltage. The voltage level should be able to shift using such as a level shifter to make the voltage for signals consistent. When a signal output is on Ethernet Board side and the voltage level of this signal is 5[V] or lower, the voltage level does not need to be shifted as an input for Control Board is 5[V] tolerant.
A pull-up or pull-down resistor should be added to Ethernet Board for the external resistor required for I2C signal, etc.

1.3.1. Ethernet Board Interface (R-Car H3 Reference Hardware)

Figure 3 shows a schematic illustrating simplified connections between Control Board and Ethernet Board for R-Car H3 Reference Hardware. Pin assignment of the connector (Ether CN) and the connected terminals are listed on Table 2.

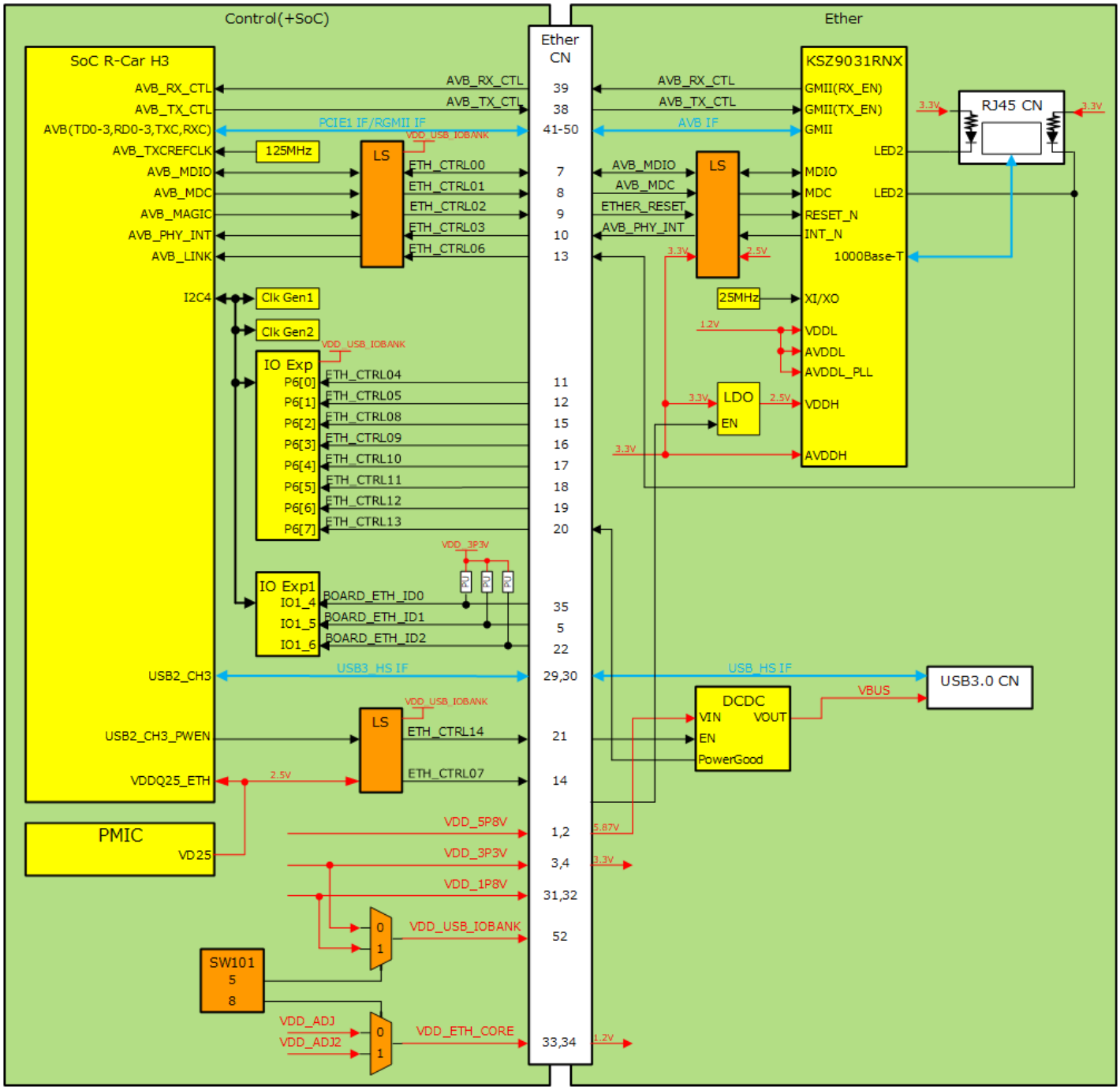


Figure 3 Connectivity between Ethernet Board and Control Board (R-Car H3 Reference Hardware)

Table 2 Connector (Ether CN) Pin Assignment and Connected Terminal in Control Board (R-Car H3 Reference Hardware)

Pin	Signal Name	Direction Control - Ether	Voltage	Connection of the control board	Description
50	AVB_RD3/PCIE1_RX1_P	<	2.5[V]	R-Car H3 "AVB_RD3" pin	RGMII RX Data3 (SoC Rx)
49	AVB_RD2/PCIE1_RX1_M	<	2.5[V]	R-Car H3 "AVB_RD2" pin	RGMII RX Data2 (SoC Rx)
44	AVB_RD1/PCIE1_RX0_P	<	2.5[V]	R-Car H3 "AVB_RD1" pin	RGMII RX Data1 (SoC Rx)
43	AVB_RD0/PCIE1_RX0_M	<	2.5[V]	R-Car H3 "AVB_RD0" pin	RGMII RX Data0 (SoC Rx)
46	AVB_RXC/PCIE1_REFCLK_P	<	2.5[V]	R-Car H3 "AVB_RXC" pin	RGMII RX Clock (SoC Rx)
48	AVB_TD3/PCIE1_TX1_P	>	2.5[V]	R-Car H3 "AVB_TD3" pin	RGMII TX Data3 (SoC Tx)
47	AVB_TD2/PCIE1_TX1_M	>	2.5[V]	R-Car H3 "AVB_TD2" pin	RGMII TX Data2 (SoC Tx)
42	AVB_TD1/PCIE1_TX0_P	>	2.5[V]	R-Car H3 "AVB_TD1" pin	RGMII TX Data1 (SoC Tx)
41	AVB_TD0/PCIE1_TX0_M	>	2.5[V]	R-Car H3 "AVB_TD0" pin	RGMII TX Data0 (SoC Tx)
45	AVB_TXC/PCIE1_REFCLK_M	>	2.5[V]	R-Car H3 "AVB_TXC" pin	RGMII TX Clock (SoC Tx)
38	AVB_TX_CTL	>	2.5[V]	R-Car H3 "AVB_TX_CTL" pin	RGMII Transmit control
39	AVB_RX_CTL	<	2.5[V]	R-Car H3 "AVB_RX_CTL" pin	RGMII Receive control
37	AVB_TXCREFCLK	-	-	NC	-
7	ETH_CTRL00	<>	3.3[V] *3	R-Car H3 "AVB_MDIO" pin	Ethernet PHY management data I/O
8	ETH_CTRL01	>	3.3[V] *3	R-Car H3 "AVB_MDC" pin	Ethernet PHY management data clock
9	ETH_CTRL02	>	3.3[V] *3	R-Car H3 "AVB_MAGIC" pin	Ethernet PHY reset (L:reset)
10	ETH_CTRL03	<	3.3[V] *3	R-Car H3 "AVB_PHY_INT" pin	Ethernet PHY interrupt (L:interrupt occurred)
11	ETH_CTRL04	<>	3.3[V] *3	IO Expander-6 bit0	Not used
12	ETH_CTRL05	<>	3.3[V] *3	IO Expander-6 bit1	Not used
13	ETH_CTRL06	<	3.3[V] *3	R-Car H3 "AVB_LINK" pin	Link activity LED status
14	ETH_CTRL07	>	3.3[V] *3	PMIC "VD25"	PHY I/O 2.5V LDO Enable (H:ON)
15	ETH_CTRL08	<>	3.3[V] *3	IO Expander-6 bit2	Not used
16	ETH_CTRL09	<>	3.3[V] *3	IO Expander-6 bit3	Not used
17	ETH_CTRL10	<>	3.3[V] *3	IO Expander-6 bit4	Not used
18	ETH_CTRL11	<>	3.3[V] *3	IO Expander-6 bit5	Not used
19	ETH_CTRL12	<>	3.3[V] *3	IO Expander-6 bit6	Not used
20	ETH_CTRL13	<>	3.3[V] *3	IO Expander-6 bit7	USB2 ch3 VBUS Power Status
21	ETH_CTRL14	>	3.3[V] *3	R-Car H3 "USB2_CH3_PWEN" pin	USB2 ch3 VBUS Enable (H:ON)
29	USB3_D_P	<>	LVDS	R-Car H3 "USB2_CH3_DP" pin	USB2 ch3 HS Data+
30	USB3_D_M	<>	LVDS	R-Car H3 "USB2_CH3_DM" pin	USB2 ch3 HS Data-

Pin	Signal Name	Direction Control - Ether	Voltage	Connection of the control board	Description
27	USB3_SS_TX0_P	-	-	NC	-
26	USB3_SS_TX0_M	-	-	NC	-
25	USB3_SS_RX0_P	-	-	NC	-
24	USB3_SS_RX0_M	-	-	NC	-
59	USB4_D_P_ETH	-	-	NC	-
60	USB4_D_M_ETH	-	-	NC	-
35	BOARD_ETH_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_4" pin, Pull-up	Ether Board ID bit0
5	BOARD_ETH_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_5" pin, Pull-up	Ether Board ID bit1
22	BOARD_ETH_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_6" pin, Pull-up	Ether Board ID bit2
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
3	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
4	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
31	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
32	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
33	VDD_ETH_CORE	>	Power:1.2[V] *1	1.2[V] output LDO	Power
34	VDD_ETH_CORE	>	Power:1.2[V] *1	1.2[V] output LDO	Power
52	VDD_USB_IOBANK	-	Power:3.3[V] *2	3.3[V] output DCDC	Power
6	GND	-	GND	GND	GND
23	GND	-	GND	GND	GND
28	GND	-	GND	GND	GND
36	GND	-	GND	GND	GND
40	GND	-	GND	GND	GND
51	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND
58	GND	-	GND	GND	GND
54	TP	-	-	NC	-
55	TP	-	-	NC	-
56	TP	-	-	NC	-
57	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (ETHER CORE voltage) on Control Board
*2: Voltage depends on the power supply switch setting (FPGA USB IO voltage) on Control Board

1.3.2. Ethernet Board Interface (Standard Reference Hardware)

Figure 4 shows the schematic of Control Board with Ether CN that connects to Ethernet Board for Standard Reference Hardware. Pin assignments of the connector (Ether CN) and the connected terminals are listed on Table 3. This schematic is applicable to R-Car H3 SoC but not for any other SoCs.

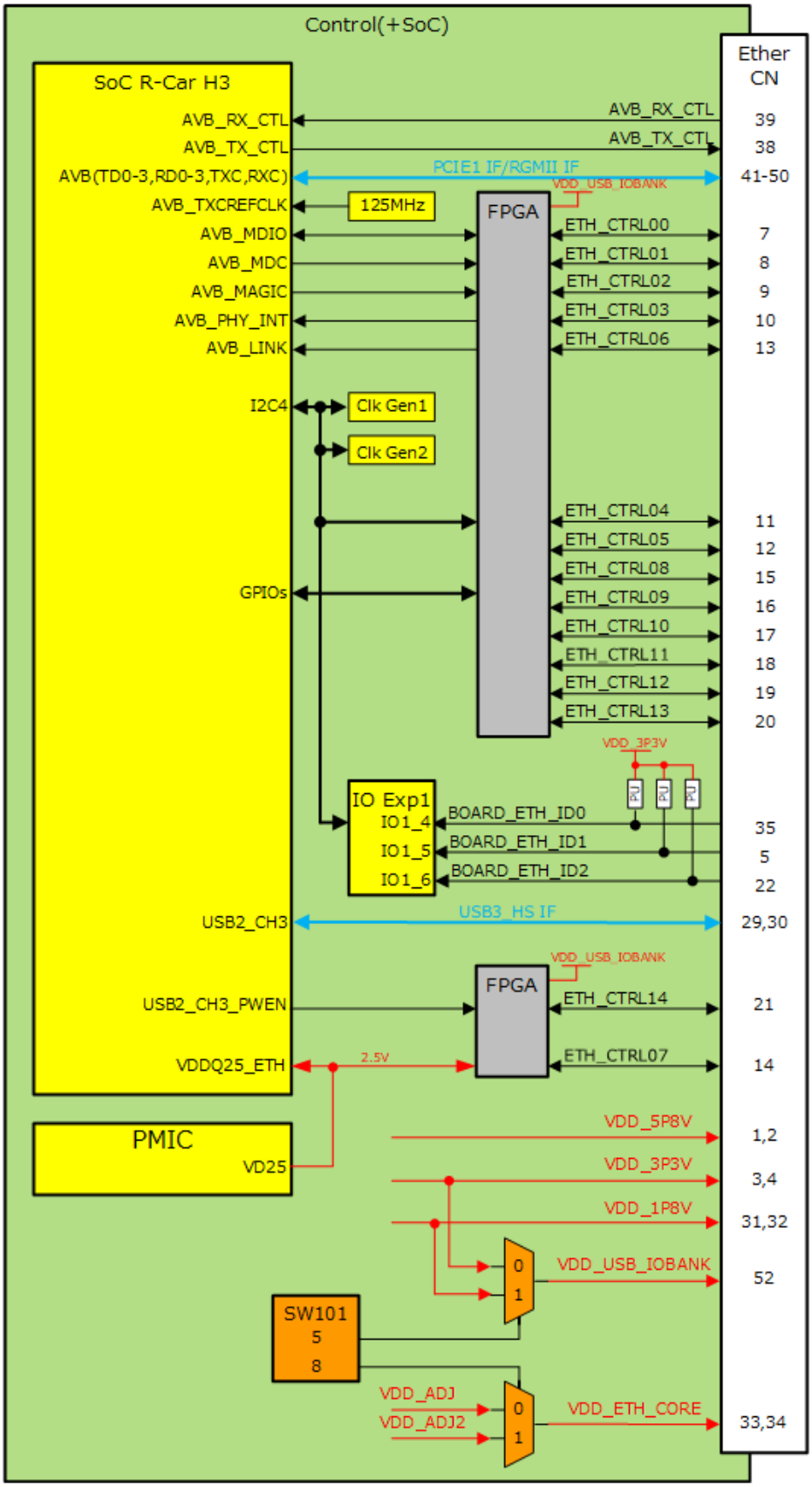


Figure 4 Connectivity between Ethernet Board and Control Board (Standard Reference Hardware)

Table 3 Connector (Ether CN) Pin Assignment and Connected Terminal in Control Board (Standard Reference Hardware)

Pin	Signal Name	Direction Control - Ether	Voltage	Connection of the control board	Description Example of use
50	AVB_RD3/PCIE1_RX1_P	<	2.5[V]/LVDS	SoC RGMII Rx Data3/PCIe ch1 Rx Data1+(SoC Rx)	RGMII RX Data3/PCIe ch1 Rx1 Data+(SoC Rx)
49	AVB_RD2/PCIE1_RX1_M	<	2.5[V]/LVDS	SoC RGMII Rx Data2/PCIe ch1 Rx Data1-(SoC Rx)	RGMII RX Data2/PCIe ch1 Rx1 Data-(SoC Rx)
44	AVB_RD1/PCIE1_RX0_P	<	2.5[V]/LVDS	SoC RGMII Rx Data1/PCIe ch1 Rx Data0+(SoC Rx)	RGMII RX Data1/PCIe ch1 Rx0 Data+(SoC Rx)
43	AVB_RD0/PCIE1_RX0_M	<	2.5[V]/LVDS	SoC RGMII Rx Data0/PCIe ch1 Rx Data0-(SoC Rx)	RGMII RX Data0/PCIe ch1 Rx0 Data+(SoC Rx)
46	AVB_RXC/PCIE1_REFCLK_P	</>	2.5[V]/LVDS	SoC RGMII RX Clock(SoC Rx)/SoC PCIe ch1 Clock+(SoC Tx)	RGMII RX Clock(SoC Rx)/PCIe ch1 Clock+(SoC Tx)
48	AVB_TD3/PCIE1_TX1_P	>	2.5[V]/LVDS	SoC RGMII Tx Data3/PCIe ch1 Tx Data1+(SoC Tx)	RGMII Tx Data3/PCIe ch1 Tx1 Data+(SoC Tx)
47	AVB_TD2/PCIE1_TX1_M	>	2.5[V]/LVDS	SoC RGMII Tx Data2/PCIe ch1 Tx Data1-(SoC Tx)	RGMII Tx Data2/PCIe ch1 Tx1 Data-(SoC Tx)
42	AVB_TD1/PCIE1_TX0_P	>	2.5[V]/LVDS	SoC RGMII Tx Data1/PCIe ch1 Tx Data0+(SoC Tx)	RGMII Tx Data1/PCIe ch1 Tx0 Data+(SoC Tx)
41	AVB_TD0/PCIE1_TX0_M	>	2.5[V]/LVDS	SoC RGMII Tx Data0/PCIe ch1 Tx Data0-(SoC Tx)	RGMII Tx Data0/PCIe ch1 Tx0 Data+(SoC Tx)
45	AVB_TXC/PCIE1_REFCLK_M	>/>	2.5[V]/LVDS	SoC RGMII TX Clock/SoC PCIe ch1 Clock-(SoC Tx)	RGMII TX Clock/PCIe ch1 Clock-(SoC Tx)
38	AVB_TX_CTL	>	2.5[V]	SoC RGMII Transmit control	RGMII Transmit control
39	AVB_RX_CTL	<	2.5[V]	SoC RGMII Receive control	RGMII Receive control
37	AVB_TXCREFCLK	<>	2.5[V]	SoC RGMII Clock	RGMII Clock
7	ETH_CTRL00	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. Ethernet PHY management data I/O
8	ETH_CTRL01	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. Ethernet PHY management data clock
9	ETH_CTRL02	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. Ethernet PHY reset
10	ETH_CTRL03	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. Ethernet PHY interrupt
11	ETH_CTRL04	<>	VDD_USB_IOBANK	FPGA	GPIO
12	ETH_CTRL05	<>	VDD_USB_IOBANK	FPGA	GPIO
13	ETH_CTRL06	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. Link activity LED status
14	ETH_CTRL07	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. LDO Enable
15	ETH_CTRL08	<>	VDD_USB_IOBANK	FPGA	GPIO
16	ETH_CTRL09	<>	VDD_USB_IOBANK	FPGA	GPIO
17	ETH_CTRL10	<>	VDD_USB_IOBANK	FPGA	GPIO
18	ETH_CTRL11	<>	VDD_USB_IOBANK	FPGA	GPIO
19	ETH_CTRL12	<>	VDD_USB_IOBANK	FPGA	GPIO
20	ETH_CTRL13	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. USB3.0 ch3 VBUS Power Status
21	ETH_CTRL14	<>	VDD_USB_IOBANK	FPGA	GPIO, e.g. USB3.0 ch3 VBUS Enable
29	USB3_D_P	<>	LVDS	SoC USB3.0 ch3 HS Data+	USB3.0 ch3 HS Data+

Pin	Signal Name	Direction Control - Ether	Voltage	Connection of the control board	Description Example of use
30	USB3_D_M	<>	LVDS	SoC USB3.0 ch3 HS Data-	USB3.0 ch3 HS Data-
27	USB3_SS_TX0_P	>	LVDS	SoC USB3.0 ch3 SS Tx Data+(SoC Tx)	USB3.0 ch3 SS Tx Data+(SoC Tx)
26	USB3_SS_TX0_M	>	LVDS	SoC USB3.0 ch3 SS Tx Data-(SoC Tx)	USB3.0 ch3 SS Tx Data-(SoC Tx)
25	USB3_SS_RX0_P	<	LVDS	SoC USB3.0 ch3 SS Rx Data+(SoC Rx)	USB3.0 ch3 SS Rx Data+(SoC Rx)
24	USB3_SS_RX0_M	<	LVDS	SoC USB3.0 ch3 SS Rx Data-(SoC Rx)	USB3.0 ch3 SS Rx Data-(SoC Rx)
59	USB4_D_P_ETH	-	-	NC	-
60	USB4_D_M_ETH	-	-	NC	-
35	BOARD_ETH_ID0	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_4" pin, Pull-up	Ether Board ID bit0
5	BOARD_ETH_ID1	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_5" pin, Pull-up	Ether Board ID bit1
22	BOARD_ETH_ID2	<	3.3[V]	IO Expander(PCA9539)-1 "IO1_6" pin, Pull-up	Ether Board ID bit2
1	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
2	VDD_5P8V	>	Power:5.87[V]	5.87[V] output DCDC	Power
3	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
4	VDD_3P3V	>	Power:3.3[V]	3.3[V] output DCDC	Power
31	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
32	VDD_1P8V	>	Power:1.8[V]	1.8[V] output LDO	Power
33	VDD_ETH_CORE	>	Power:1.2[V] *1	1.2[V] output LDO	Power
34	VDD_ETH_CORE	>	Power:1.2[V] *1	1.2[V] output LDO	Power
52	VDD_USB_IOBANK	-	Power:3.3[V] *2	3.3[V] output DCDC	Power
6	GND	-	GND	GND	GND
23	GND	-	GND	GND	GND
28	GND	-	GND	GND	GND
36	GND	-	GND	GND	GND
40	GND	-	GND	GND	GND
51	GND	-	GND	GND	GND
53	GND	-	GND	GND	GND
58	GND	-	GND	GND	GND
54	TP	-	-	NC	-
55	TP	-	-	NC	-
56	TP	-	-	NC	-

Pin	Signal Name	Direction Control - Ether	Voltage	Connection of the control board	Description Example of use
57	TP	-	-	NC	-

*1: Voltage depends on the power supply switch setting (ETHER CORE voltage) on Control Board

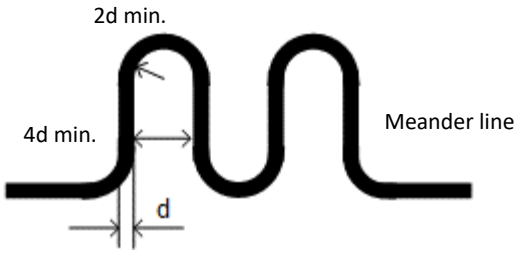
*2: Voltage depends on the power supply switch setting (FPGA USB IO voltage) on Control Board

1.4. Board Layout Consideration

Due to LVDS lines on Control Board, traces on Ethernet Board need to be designed in accordance with the following restrictions:

PCI-Express Differential Signal

- Trace Length Matching: Difference between a differential signal pair (+and –) must be 0.1[mm] maximum.
- Difference between an average length of a clock pair (average of + signal and – signal)/a data signal pair : 0.1[mm] maximum.
- Maximum Trace Length : 30[mm]
- Differential Impedance : 85[Ω](85[Ω] on Control Board side)
- Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically.
- Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be at least twice the width of the trace. The gap between the meander traces should be at least four times the trace width.



USB High-Speed Differential Signal

- Trace Length Matching: Difference between a differential signal pair (+and -) must be 0.5[mm] maximum.
- Maximum Trace length : 50[mm]
- Differential Impedance : 90[Ω](90[Ω] on Control Board side)
- Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically.
- Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be twice the width of the trace. The gap between the meander traces should be at least four times the trace width. (as shown above)

USB-SuperSpeed Differential Signal

- Trace Length Matching: Difference between a differential signal pair (+and –) must be 0.1[mm] maximum.
- Maximum Trace Length : 30[mm]
- Differential impedance : 90[Ω](90[Ω] on Control Board side)
- Spacing between adjacent signal traces should be at least 4 times the width of the trace. The length of trace running parallel must not exceed 5 [mm] horizontally or vertically (e.g. stripline).
- Minimize the use of stubs. If used, the maximum length should be 1 [mm].
- For meander trace routing, the curve needs to be arc-shaped, and the radius (of internal diameter) should be twice the width of the trace. The gap between the meander traces should be at least four times the trace width. (as shown above)

Power Supply

- Comply with power supply requirements (impedance property, etc.) of the device to connect.
  If the requirements are unavailable, trace width and the number of vias should be determined to restrict the temperature rise at +10[℃] or less when maximum load is applied at each voltage considering specifications (copper thickness, via diameter, etc.) of the board.

Miscellaneous

- Comply with general design rules, such as parallel trace avoidance, GND guard, trace width, impedance, trace length, etc.
- Care needs to be given for bus lines such as MII when connecting to a PCI-Express connector terminal.

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